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OBJECTIVE:

To reestablish my technical career.

SUMMARY:

I have hosted myself, https://softglue.com & have experience with LAN and WAN networks, Lotus Notes, Lotus / Domino servers, UNIX, C, SQL, Microsoft Visual Basic, Lotus Notes Visual Basic & Windows Powershell IT script, License holder of Visual Studio 2022 and focus on Visual Basic 2022 .net, CSS, HTML & JavaScript scripting. Also since 8/2021, have a remote web hosting security based wordpress website, https://softglue.net developed & maintained by me.

I have 15 years of face-to-face customer interfacing with a team oriented frame of mind, and a winning and leadership attitude. Customer interfacing has included answering customer questions through written and verbal forms, on site customer training, solving tough customer problems internally and on site, and communicating the results to all levels of management.

Managed component product monitor and qualification programs with budget responsibilities. Also used Failure Mode Effects Analysis (FMEA) to help improve product and process robustness. Have done some business travel internationally

RELIABILITY ENGINEERING EXPERIENCE:

1. Experience performing reliability testing including Static, Dynamic and Vector Driven Operating Life Test at 125C and 150C accelerated testing, Mechanical Stress Tests such as Temperature Cycle, and Thermal Shock, and Environmental Tests such as Temperature Humidity Bias (85C/85%RH), Highly Accelerated Stress Test (135C/85%RH) , Non-Bias Pressure Pot (121C, 100%RH, 1Atm.

2. Human Body Model ESD testing at 2000V, and F.A. root cause of I/O cells. Charge Device Model / Zero ohm ESD testing at 200V, and F.A. root cause of I/O cells.

3. Reliability Statistical Analysis using lognormal and Weibull with Chi2 distributions hand charting experience and hand calculations of standard distribution sigma, Weibull statistic, and hand calculations of activation energy based of reliability lognormal split matrix. Have direct SPC statistic experience with JMP. Familiar with accelerated test models such as Failure in Time (FITS) as a function of temperature and activation energy. Familiar with the power law failure rate distribution model of thermal stress. Familiar with failure rate model of humidity bias testing. It is a function of both the operating life failure rate, and an acceleration of electric corrosion of the lead frame, bond pad and unsealed pin whole passivation.

4. Familiar with Failure Analysis techniques (Optical Microscopy (EMI), X-ray/CT, Scanning Electron Microscopy (SEM), focused ion Beam (FIB), and E-Beam analysis, and the ability to use failure analysis methodology to derive a root cause of failure such as micro probing, fault isolation bench analysis, liquid crystal, parallel lap polishing, chemical etch back. Cross section, and potting cross section, and plasma etch back.

5. Completed official course work at National Semiconductor on Design of Experiments. Have experience with factorial analysis 2^2 and 2^3 factorial, and break down of 2^4.

6. Failure Modes and Effects Analysis is defined as the sum of all failure modes with the highest probabilities listed first, and are analyzed first, and all activation energies must be known.

7. Performed wafer level reliability testing of time dependent dielectric breakdown, hot carrier and electromigration (EM) reliability test matrix and calculated their reliability statistics using lognormal distribution analysis. Also, designed my own EM minimum geometry metal line width test structures.

RELEVANT SKILLS:

Standardized companywide reliability test, reliability test hardware, ESD and Latch-up methodologies and requirements.

Written many reliability specs and reliability test hardware data sheet notes.

1. 25 years of visual basic API applications and IT client VBscript development.
2. 7+ years of Microsoft Powershell IT client development.
3. 25 years of visual basic EXCEL macro development
4. 4 years of general Microsoft server administration of DNS, DHCP and IIS web servers.
5. 8 years of Lotus notes development
6. 4 years of Lotus Domino Administrator experience on Windows NT OS platform in both network client and web administration
7. Have performed windows 7 migration to windows 10 by both the windows update and down loading the ISO, and updated all drivers afterword's, and tested key apps to ensure they startup correctly.

WORK EXPERIENCE:

07/12-Present SoftGlue

Software Developer & Owner

Personal Venture. https://softglue.net is security based WORDPRESS web site completely owned, written and maintained by me. It used custom email and commit blogging CSS, HTML & hava script controls written by me. The word press pages are both wordpress GUI & wordpress PHP script written & maintained by me. I fully understand how to develop & use the wordpress website database application. I can configure and program any wordpress plugin so long as I have access to its application documdents.

Develop vb.net applications & website CSS, HTML & JavaScript page plugins. Developed a Visual powershell / C script compiler in allocated reserved RAM memory. Seeking funding for the venture.

San Jose, Ca

1. Developed personal visual basic and Microsoft Powershell client IT scripts.

2. All softglue.net posted applications are unique and are **DevOp automated applications** using exactly the same API controls to the exact same external control application with different application specific input to control the applications access and licensing security. It is minor development to add any new application to use these controls, even a third part application if the internal API is compiled with application threaded input communication. The applications posted use this API as an internal API for maximum application startup socket layer security.

3. Also have 25 years in developing visual basic applications and using VB APIs and 7 years with C script. Also, have written personal APIs to the windows API standards. I have written my own non published windows APIs and have written my own documents on how to use them.

4. Self-proctorship SoftGlue, Software Tools & Virtual Network Company – www.SoftGlue.net
   Established 8/10/2021, License# 033675
   Productized six offered software tools using software Dev Ops and automation.
   1) API Thread Demo
   2) Application Extension
   3) Encrypted Syntax Translator
   4) RGB Dynamic Color Palette
   5) Viasual Powershell full system application demo
   6) Visual Powershell Web Links

07/22-02/23 The Home Depot

San Jose, Ca

ProXTRA Associate

Sold construction materials to construction contractors.

02/17-09/19 Goodwill Silicon Valley

San Jose, Ca

E-Commerce Re-compute Technician

1. Refurbish personnel computers, laptops, cell phones, and tablets.

12/05-4/06 Frys Electronics

Sunnyvale, Ca

Computer Service Technician

1. Assisted customers with computer and software problems over the counter.
2. Repaired desktop and laptop computers by changing broken power connectors.
3. Cleaned store computers and printers.

09/05-11/05 Platinum Consultants

San Jose, Ca

Parts Specialist

Space Systems / Loral

1. Reviewed satellite parts list quality compliance, supported resolution of parts problems
2. Coordinated and resolved supplier issues, generated parts documents, and performed data review.
3. Development an Excel visual basic macro that supported database records extraction into Excel.
4. Development a curve tracer data EXCEL macro engineering analysis tool.
5. Perfumed system module level failure analysis.

01/03-12/05 SoftGlue

Software Developer & Owner

San Jose, Ca

1. Developed personal visual basic and Microsoft Powershell client IT scripts as a leaning aid. Also have 25 years in developing visual basic applications and using VB APIs and 7 years with C script. Also, have written personal APIs to the windows API standards. I have written my own non published windows APIs and have written my own documents on how to use them.

01/01–11/02 Schlumberger

San Jose, Ca

Applications Engineer

1. Developed applications related to the company's SUN Solaris based e-beam, OptiFib, and Pico Second Circuit Analysis equipment.
2. Carried out customer related technical operations, including bug verification and new product release and validation testing. See Applications Engineering Cover letter.
3. Provided development support for the company's Clear Quest bug tracking database.
4. Successfully represented new and existing business and existing business for Schlumberger as applications support.

1998-2000 C-Cube Microsystems

Milpitas, Ca

Senior Reliability Engineer

1. As a key member of the ESD task force team, successfully managed the testing and development of product level ESD and Latch-up improvement Programs.
2. Performed product qualifications and failure analysis on VCD, DVD, and Encoder products.
3. Wrote reliability requirements specification. Wrote an ESD requirements specification.
4. Managed subcontractor qualification failure analysis labs.
5. Developed a MS Access reliability engineering data bases.
6. Design reliability system level vector driven Operating Life test boards for asynchronous VLSI digital logic devices, and THBT boards, and wrote the data sheets.

1994-1998 Orbit Semiconductor

Sunnyvale, Ca

Senior Reliability Engineer

1. Successfully managed the company's Reliability Engineering Group, which oversaw the development of the Qualification, and Product Monitoring programs.
2. One direct report.
3. Successfully created and ran a real-time wafer fab manufacturing Statistical Process Control (SPC) program, subsequently maximizing the utilization of Orbit Semiconductors Work in Progress tracking system. Additionally replaced all SPC paper charts with online computer representations providing companywide availability.
4. Performed critical RMA problem resolutions.
5. Facilitated company meetings as SPC chair.
6. Acted as a customer sales liaison for reliability, by presenting them to potential customers, writing on demand reliability data analysis reports for wafer fab and ENCORE gate array products and corporate clients.
7. Wrote reliability requirements specification for wafer fab and ENCORE gate array products.
8. Designed a physical design degradable resistor and a current funnel interface layout for performing electromigration. Wrote a process monitor (PCM) statistical data analysis program by PCM module.
9. Developed a Lotus Notes reliability engineering database.
10. Ran Orbit's Wafer Level Reliability Program. This included, WLR equipment procurement, on time and meaningful data reporting for wafer fab and business needs, designed a physical design degradable resistor electromigration test structure, WLR chip layout for efficient wire bonding, gate oxide testing, electormigration testing, and hot carrier testing.
11. Managed Orbit's reliability-engineering budgets for four years.
12. Successfully represented new business and existing business for Orbit Semiconductor.
13. Design reliability system level dynamic driven Operating Life test boards for asynchronous ENCORE gate array digital logic devices, and THBT boards, and wrote the data sheets.

1988-1994 National Semiconductor

Santa Clara, Ca

Senior Reliability Engineer

1. Conducted manufacturing qualifications on newly developed products.
2. Chemical lab certified and performed root cause failure analysis.
3. Led the ISO preparation team for the reliability department supported by familiar ISO9000 philosophies yielding operationally profitable results.
4. Design reliability system level vector driven Operating Life test boards for asynchronous VLSI digital logic devices, and THBT boards, and wrote the data sheets.

EDUCATION:

1986 University of California Riverside Bachelor of Science, Physics

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General Summary Cover:

While my direct experience resides primarily within semiconductor quality and reliability, I have worked directly with all aspects of semiconductor backend in wafer fab, and end product; such as product engineering, test, SPC, wafer level reliability (WLR), new and existing business customers, new business audits, new product introduction processes such as product definition, design phase, tape out phase, manufacturing phase (wafers out, and device assembly), and production test development (temperature testing, and test fixture development) etc. I also have experience with LAN and WAN networks, UNIX, C, SQL, Visual Basic, and HTML scripts.

As an example of my technical and organizational skills, I created and ran Orbit's reliability program for four years. The program included a real time SPC fab program, end product monitor program, new process and customer product qualification programs which supported sales and marketing QA/R issues.

Orbit's reliability program also included a comprehensive wafer level reliability program, which supported new process development for both new process technology nodes and major changes to existing fab processes, which I created and ran. For example, I purchased all necessary capital equipment, and designed my own minimum geometry aluminum alloyed based metal film electromigration structures, which I used to successfully evaluate and qualify new aluminum film based processes for Orbit Semiconductor. See image below. The elecromigration test structure is a copy writeable, possible patentable degradable parametric resister design. I look forward in hearing from you to discuss a career move to your company.

Regards,

Mark

Electromigration Test Structure:

The electromigration design was a redesign of the industry standard four point serpentine structure to test metal film metal line widths < 1um in width. The designs in Diagrams 1 & 2 worked successfully for a 0.8um metal line width film for a 2 metal, 1 poly 0.8um design rule planerized CMOS process [3]. Up until the design in this study, approximately 1.2um metal film width lines was the smallest metal film width that could be successfully stressed without fusing the electromigration (EM) line at the active EM line to device pad interface due to extremely large pad to active metal line aspect ratios of approximately >= 65. For CMOS processes >= to about 0.5 microns design rule, pad widths approach 65 micron squares. It was outside the electrical & physical design rules to design on silicon active devices in this manner. However, EM testing was done on metal film lines with relaxed design rules and failed for design rule fusing for metal line connection aspect ratios >= 65. The metal film process used in this study used about a 65um square pad and so it was not possible to bias a 0.8um metal width film line directly to a 65um square pad with current source bias conditions of 200mA to 250mA without fusing as is in reference (3) of this paper.

The problem was solved once the device physics was understood that no testability of less than 1.2um metal widths was fusing caused by exceeding the natural gage rating of the metal film at the pad to metal film interface and not failing to uphold Kirkoff's laws of power distribution. Diagram 1 is the anti-fuse new active device design interconnect, designed circa 1996 to the industry standard four point serpentine structure of Diagram 2. U.S. patents pending. The ant-fuse current funnel or electron escape hatch tapers as current passes and therefore upholds the 0.8um CMOS process physical and electrical design rules for EM stress testing in reference (3). As a result, the new electromigration structure design shown in Diagram 2 worked and yielded expected electromigration test results with a tight standard deviation (sigma) distribution, accurately predicting the planerized 0.8um one poly, 2 metal alloy (TiNitride-Al, 1%CU, 0.5 Si-TiNitride) sandwich metal film life time for production. Kirchhoff's circuits law [1] had no impact on the physical design of current funnel EM structure interconnect successful circuits working of the current funnel gauge theory anti fuse without fusing under high electrical power loads per unit metal line volume.

Current Funnel / Electron Escape Hatch & 0.8um Metal Width Electromigration Test Structure

Diagram 1

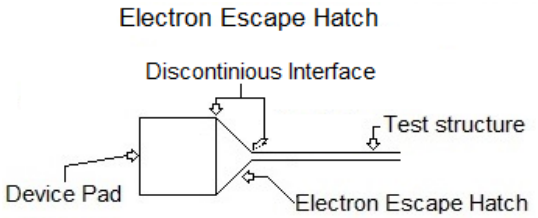

Diagram 2